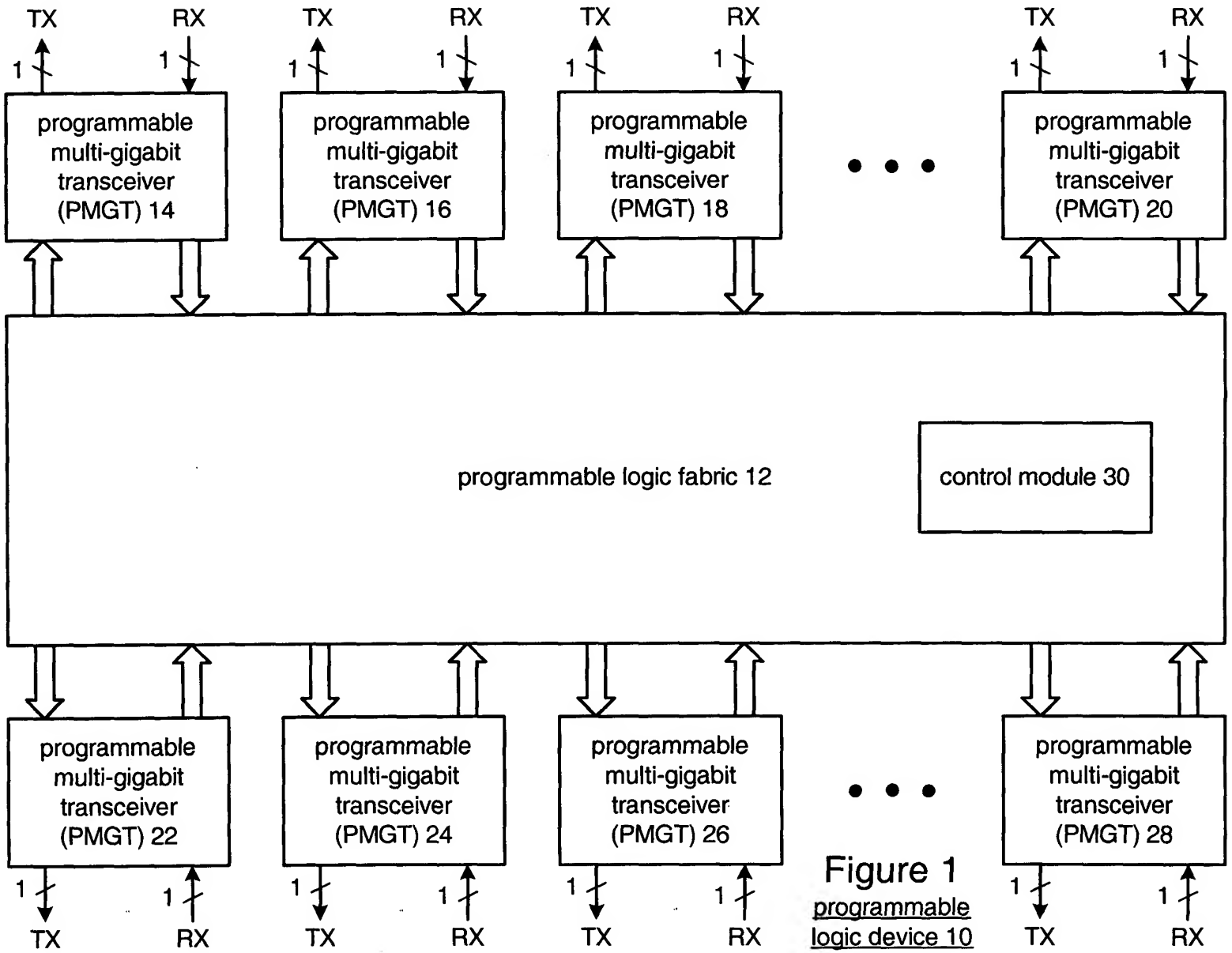


Figure 1
programmable logic device 10

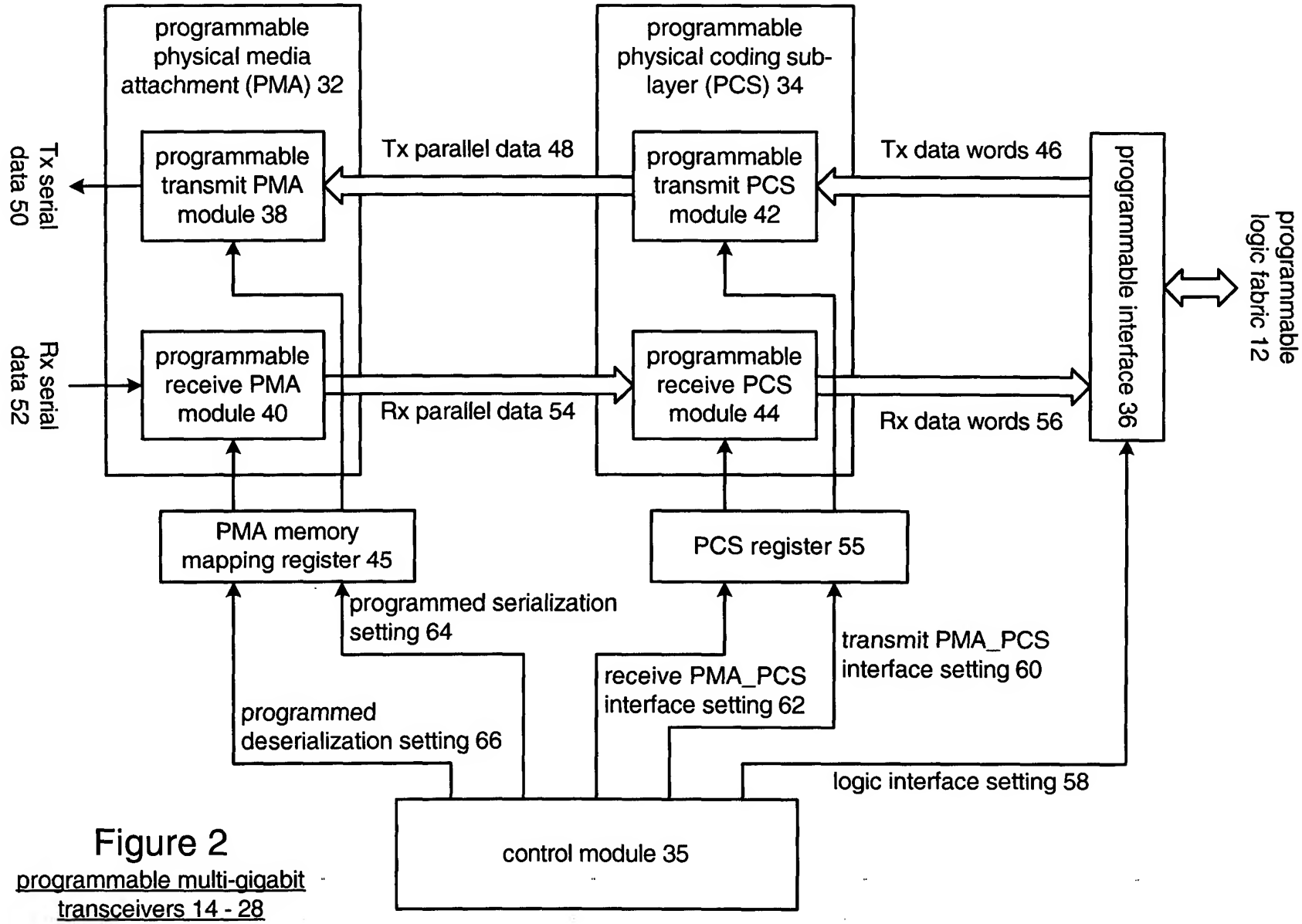


Figure 2

programmable multi-gigabit transceivers 14 - 28

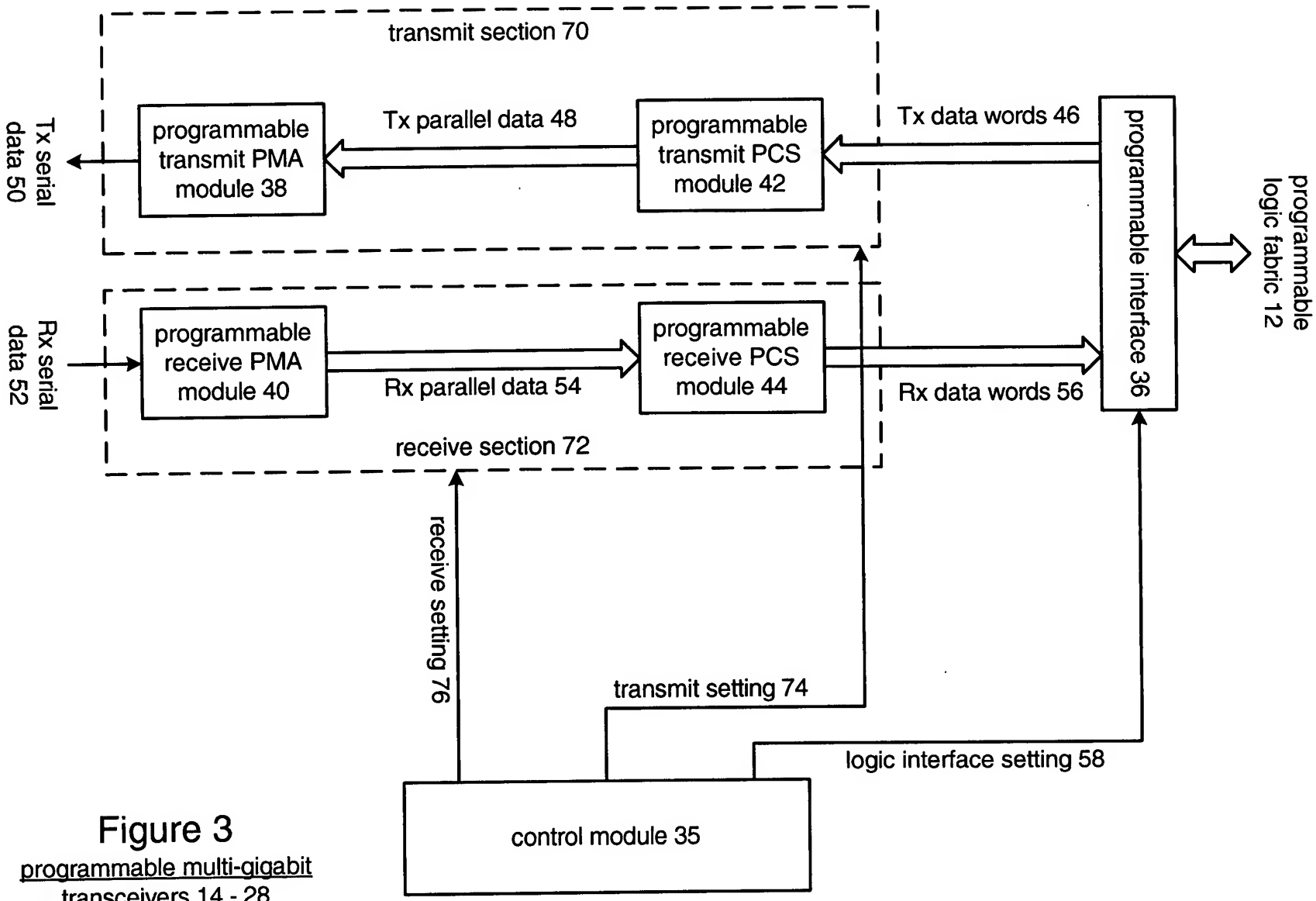


Figure 3
programmable multi-gigabit transceivers 14 - 28

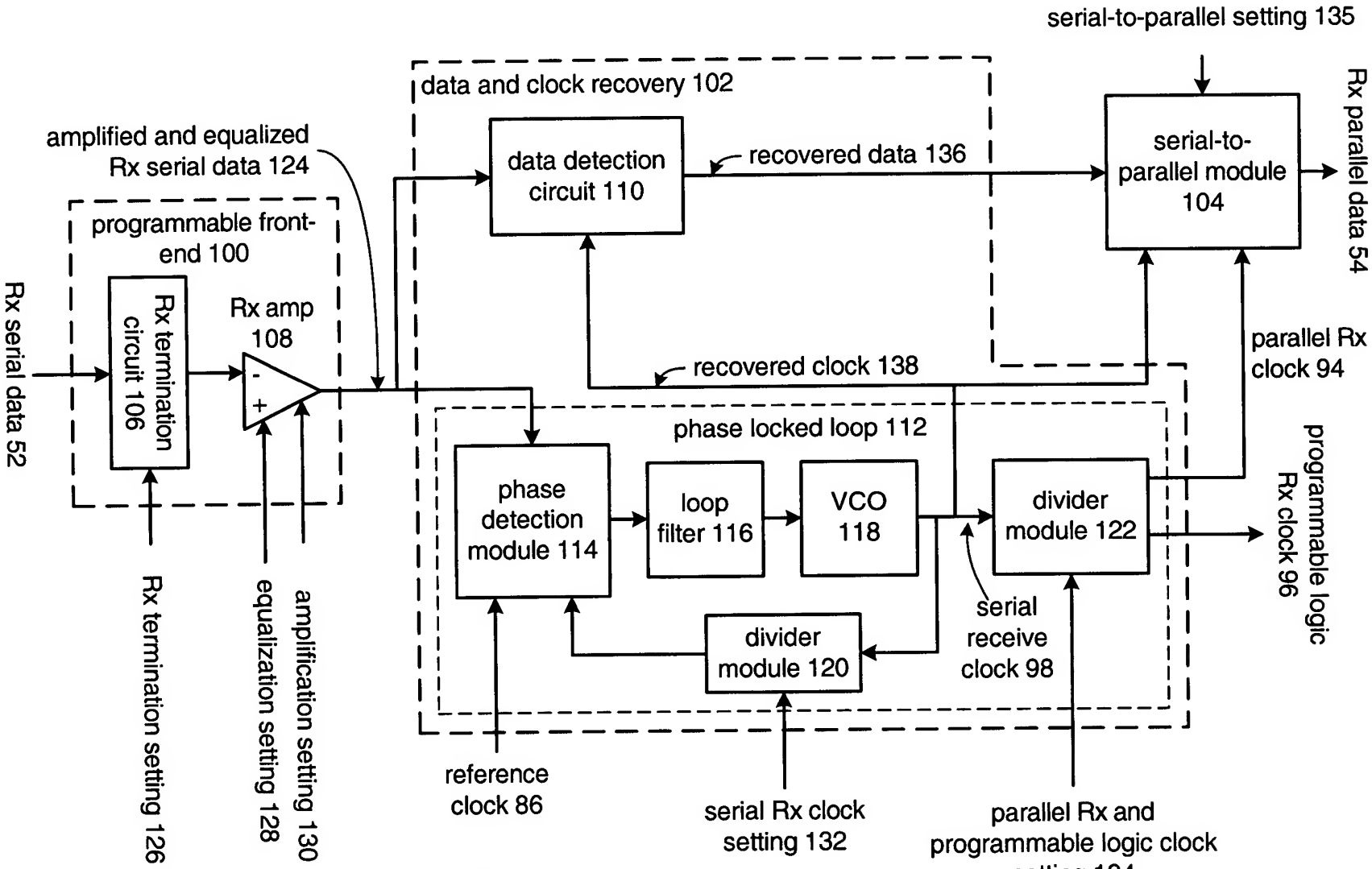


Figure 4A

programmable receive
PMA module 40

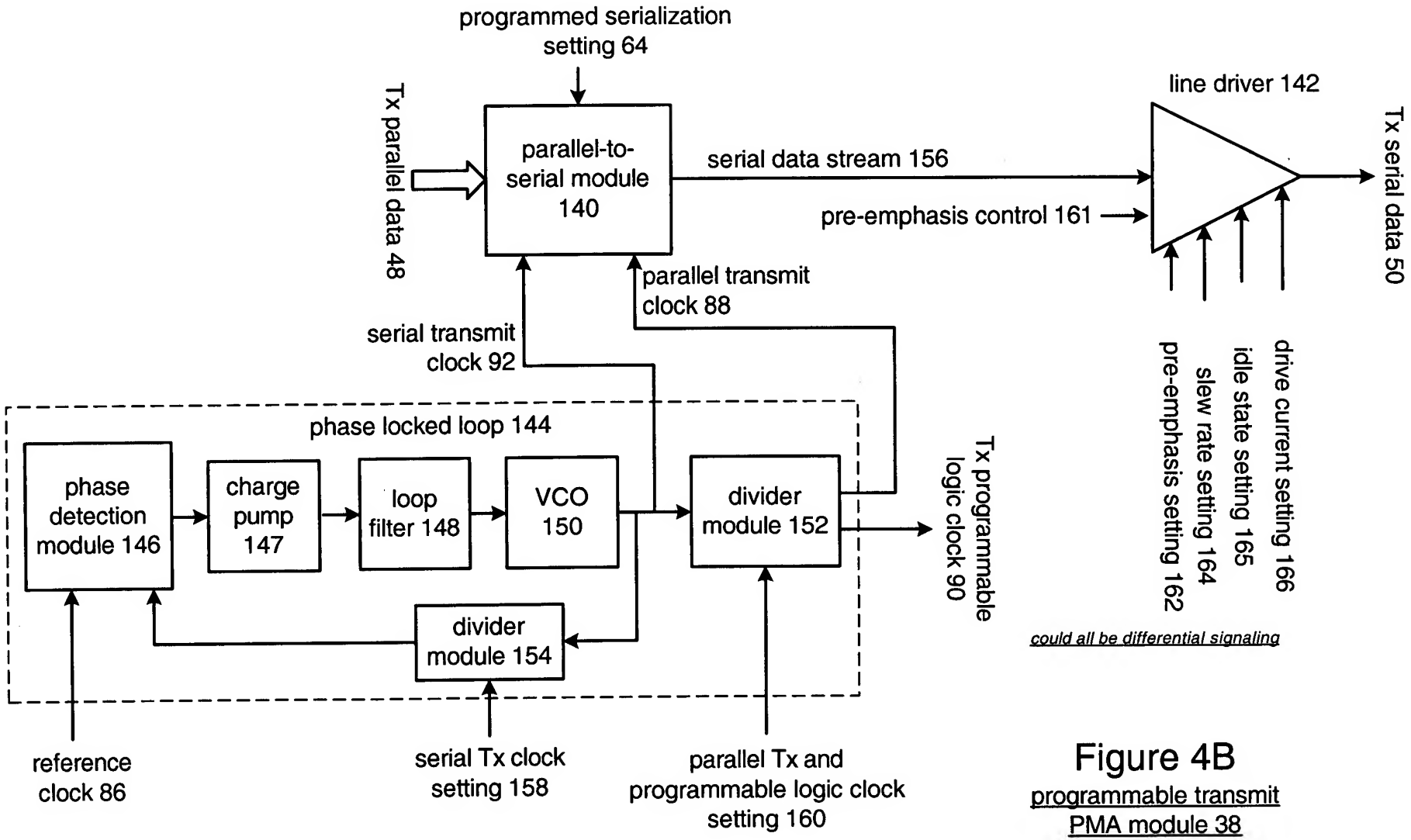


Figure 4B
programmable transmit PMA module 38

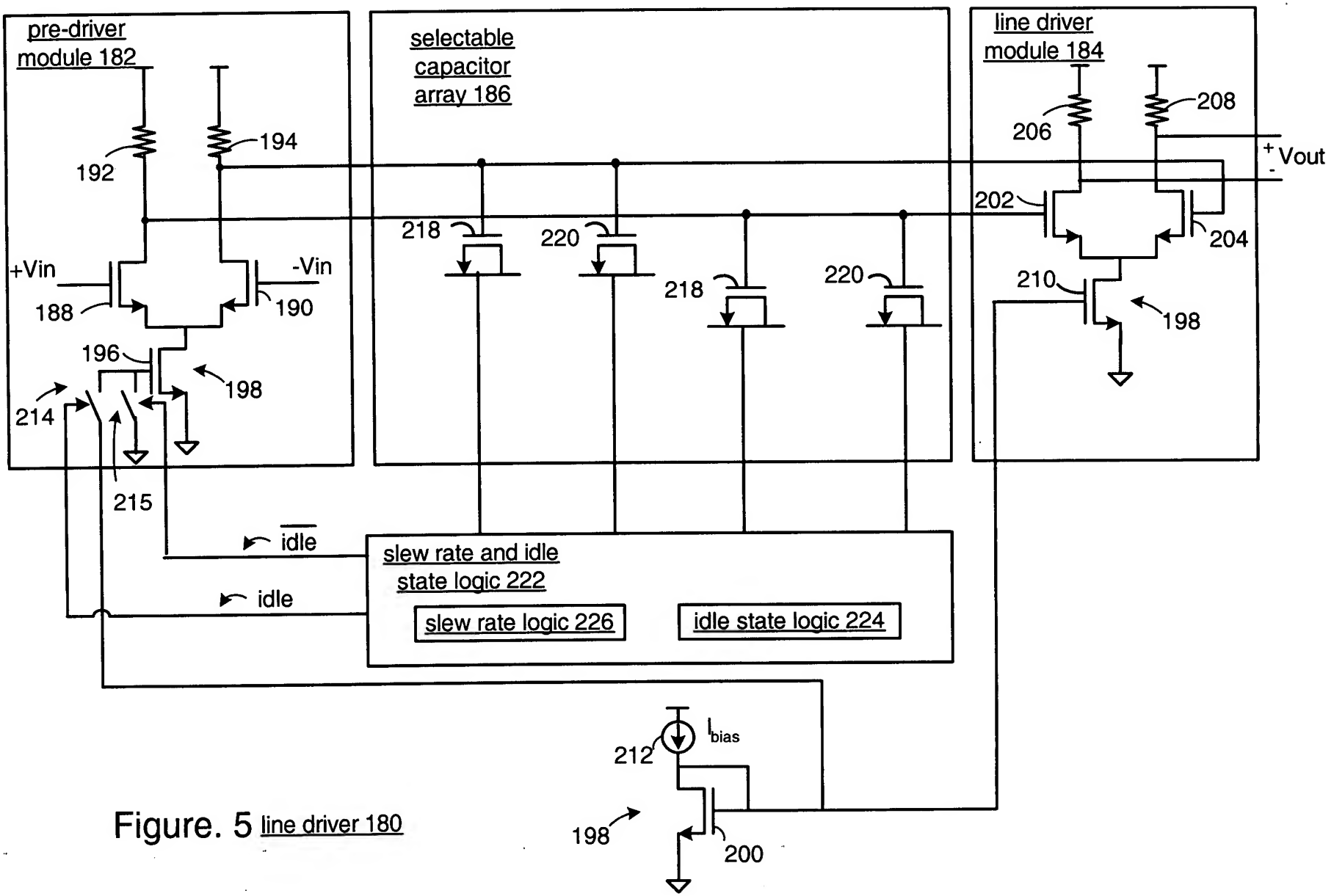


Figure. 5 line driver 180

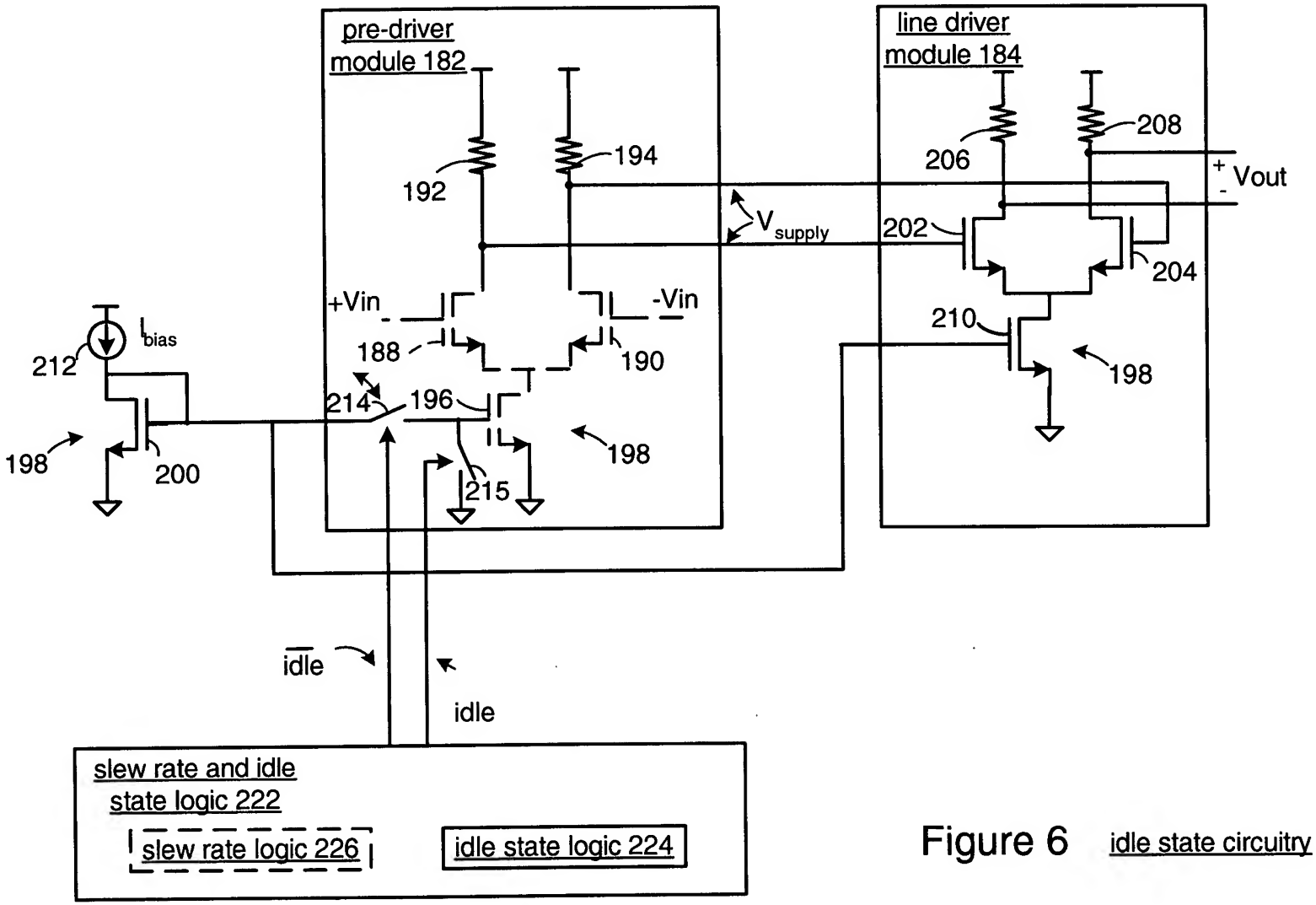


Figure 6 idle state circuitry

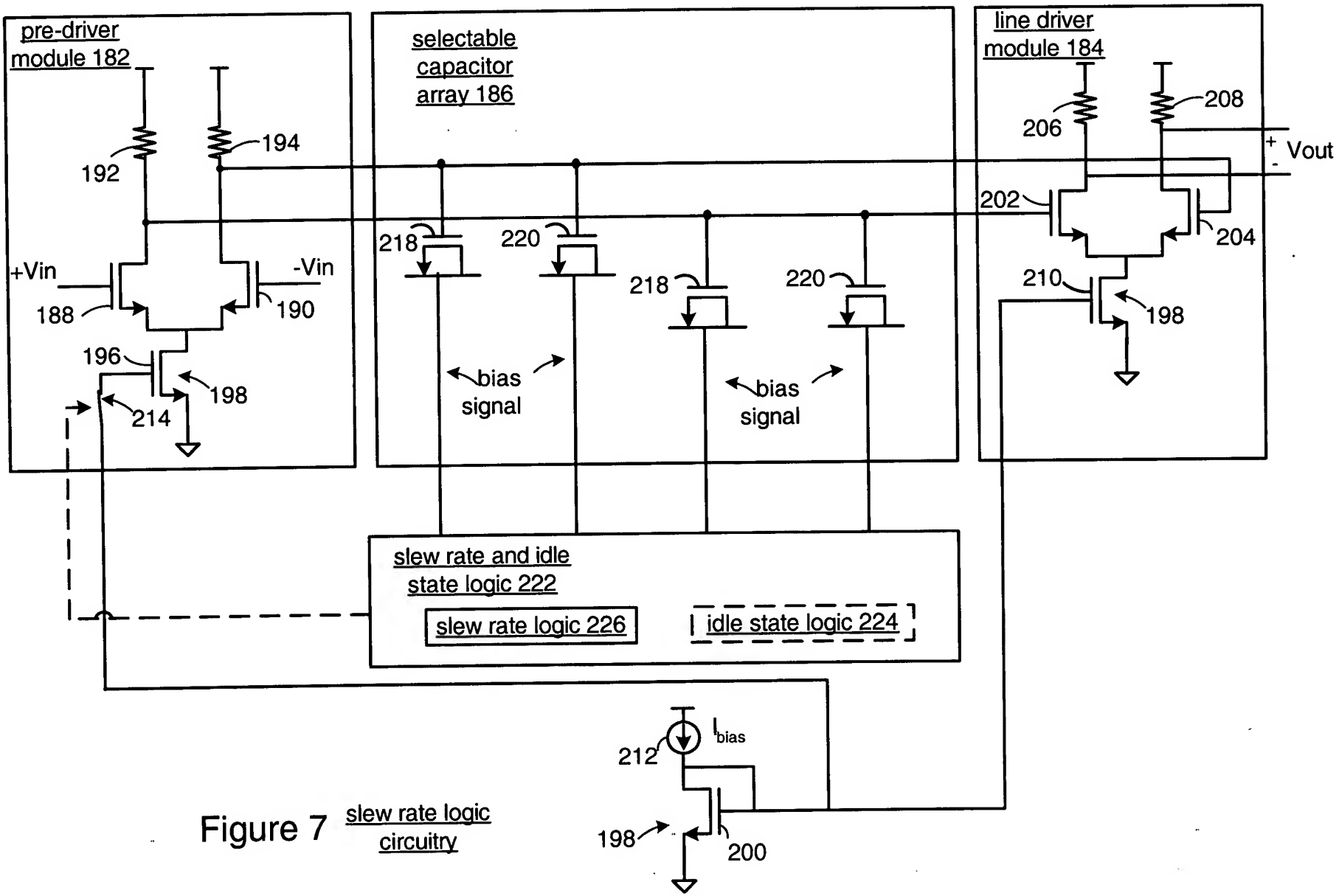
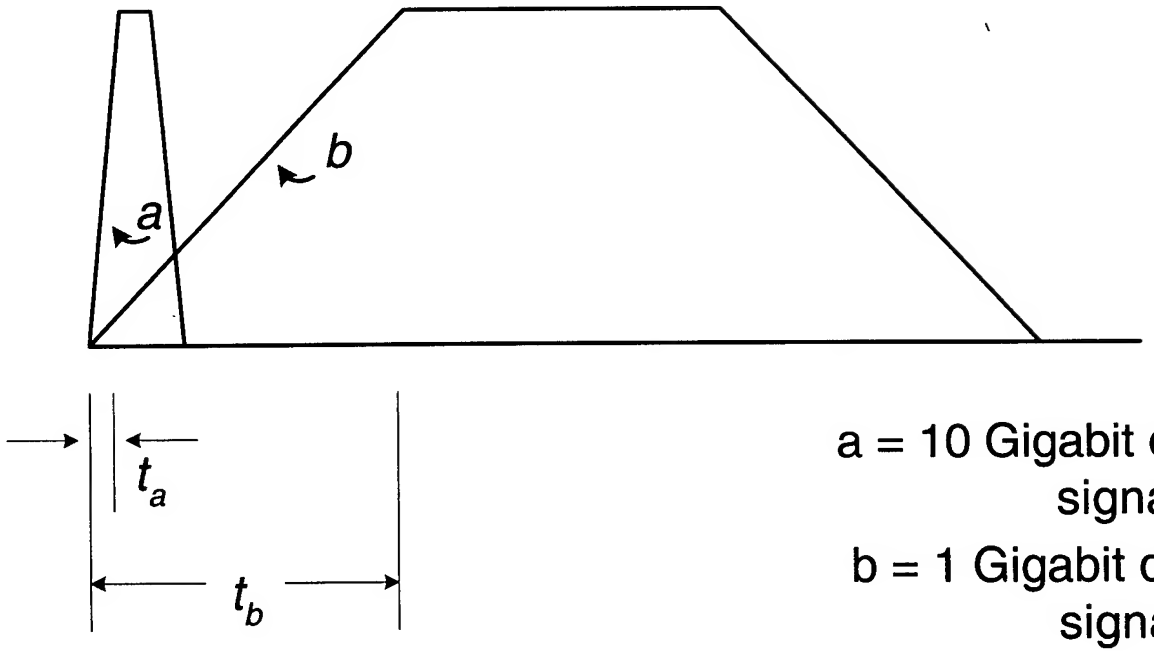


Figure 7 slew rate logic circuitry



a = 10 Gigabit data stream signal

b = 1 Gigabit data stream signal

Figure 8

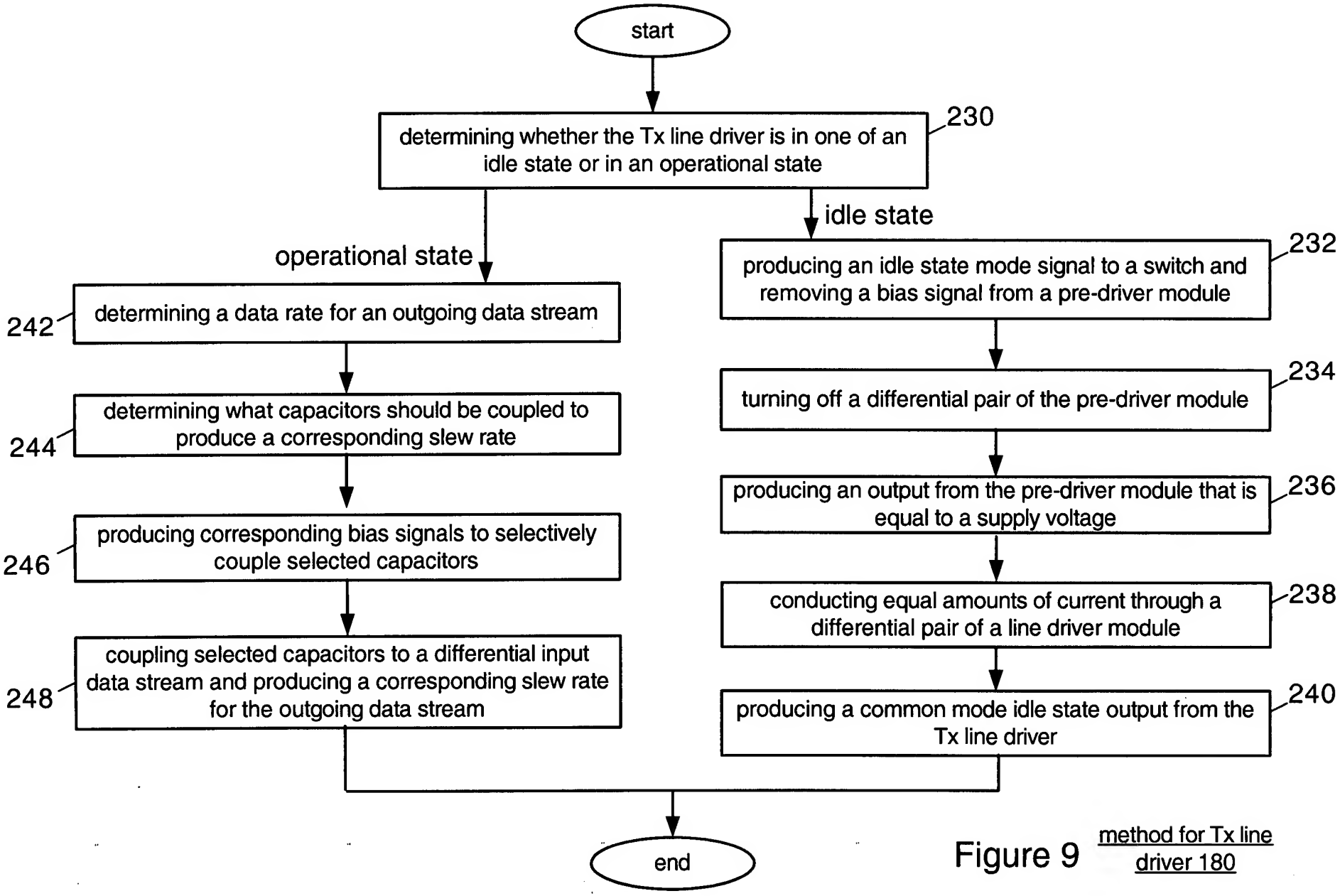


Figure 9 method for Tx line driver 180